Ordering number: EN 4952

Monolithic Linear IC

LA7578N

IF Signal Processing (Super PLL-II VIF + SIF) Circuit for TVs and VCRs

Overview

The LA7578N is an intercarrier-type VIF + SIF IC that supports excellent sound quality and image quality.
The pin assignment of the LA7578N is identical to that of the LA7577N, allowing the LA7577N to be used for split systems while the LA7578N is used for intercarrier systems. In addition, the LA7578N suppresses Nyquist buzz interference by using a PLL detection system with a buzz canceller in order to provide the best sound quality possible.

Functions

[VIF Block]

- VIF amplifier
- VCO
- APC filter
- B/W NC
- AFT
- IF AGC
- PLL detector
- Equalizer amplifier
- Lock detection
- RF AGC
- APC detector
- Buzz canceller

[SIF Block]

- Limiter amplifier
- FM quadrature detector

[Mute]

- Audio mute (pin 2)
- IS-15 switch (pin 13)
- AV mute (pin 4)

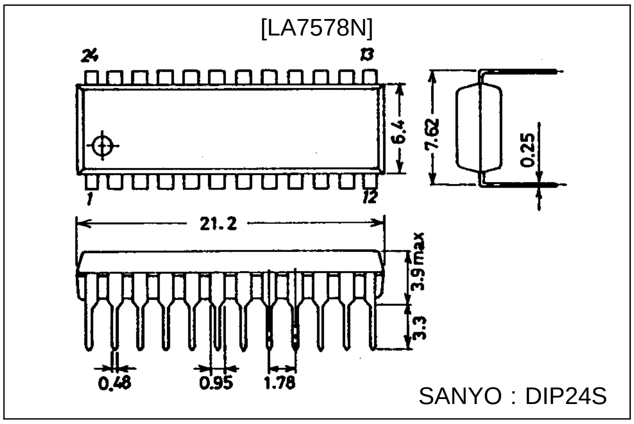
Features

- Excellent buzz and buzz-beat characteristics due to PLL detection system with buzz canceller.
- Built-in APC time constant switch.
- Duplicate time constant system suited for high-speed AGC.
- Excellent DG and DP characteristics.
- RF AGC adjustment is simple.

Package Dimensions

unit : mm

3067-DIP24S



Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		13.8	V
Allowable power dissipation	Pd max	Ta ≦ 50 °C	1200	mW
Circuit voltage	V_3, V_{13}		V_{CC}	V
	V_{14}		V_{CC}	V
Circuit current	I_1		–1	mA
	I_{17}		–10	mA
	I_{21}		–3	mA
	I_{10}		3	mA
Operating temperature	Topr	Note 1	–20 to +70	°C
Storage temperature	Tstg		–55 to +150	°C

Note : The current that flows into the IC is positive (no signal); the current that flows out of the IC is negative.
Note 1 : –20 to +75 °C at V_{CC} = 9 V

Operating Conditions at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		9 or 12	V
Operating supply voltage range	V_{CC} op		8.2 to 13.2	V

Note:
- Always turn on the protective resistance when drawing a line directly out from the IC at usage. (Pins 2, 11, 12, etc.)
- A capacitor with favorable humidity characteristics should be used for pin 13. (ex. OS capacitor)
- Pin 8 (NC) should always be open.

Operating Characteristics at Ta = 25 °C, V_{CC} = 12 V

Parameter	Symbol	Conditions	min	typ	max	Unit
[VIF Block]						
Circuit current	I_9	V_{13} = 5 V, S1 = ON	42	48	57	mA
No-signal video output voltage	V_{21}	V_{13} = 5 V, S1 = ON	6.6	7	7.4	V
Maxinum RF AGC voltage	V_{10H}	V_{13} = 7 V, S1 = OFF	10.6	11	11.4	V
Mininum RF AGC voltage	V_{10L}	V_{13} = 7 V, S1 = ON		0	0.5	V
No-signal AFT voltage	V_{14}	V_{13} = 5 V, S1 = ON	3.0	5.9	8.0	V
Input sensitivity	Vi	S1 = OFF	33	39	45	dB/µV
AGC range	GR	S1 = ON	60	66		dB
Maximum allowable Input	Vi max	S1 = ON	100	105		dB/µV
Video output amplitude	V_O (video)	S1 = ON	1.95	2.25	2.55	Vp-p
Output S/N	S/N	S1 = ON	49	55		dB
Sync signal tip voltage	V_{21} (tip)	Vi = 10 mV, S1 = ON	4.15	4.45	4.75	V
920 kHz beat level	I_{920}	P = 0, C = –4 dB, S = –14 dB, S1 = ON	37	43		dB
Frequency characteristics	fc	P = 0, S = –14 dB	6	8		MHz
Differential gain	DG	Vi = 10 mV, 87.5% mod, fp = 58.75 MHz		3	6	%
Differential phase	DP			2	5	deg
Maxinum AFT voltage	V_{14H}		11	11.5	12	V
Mininum AFT voltage	V_{14L}		0	0.4	1.0	V
White noise threshold voltage	V_{WTH}		8.9	9.3	9.7	V
White noise clamp voltage	V_{WCL}		5.3	5.7	6.1	V
Black noise threshold voltage	V_{BTH}	S1 = ON	3.4	3.7	4.0	V
Black noise clamp voltage	V_{BCL}	S1 = ON	5.3	5.7	6.1	V

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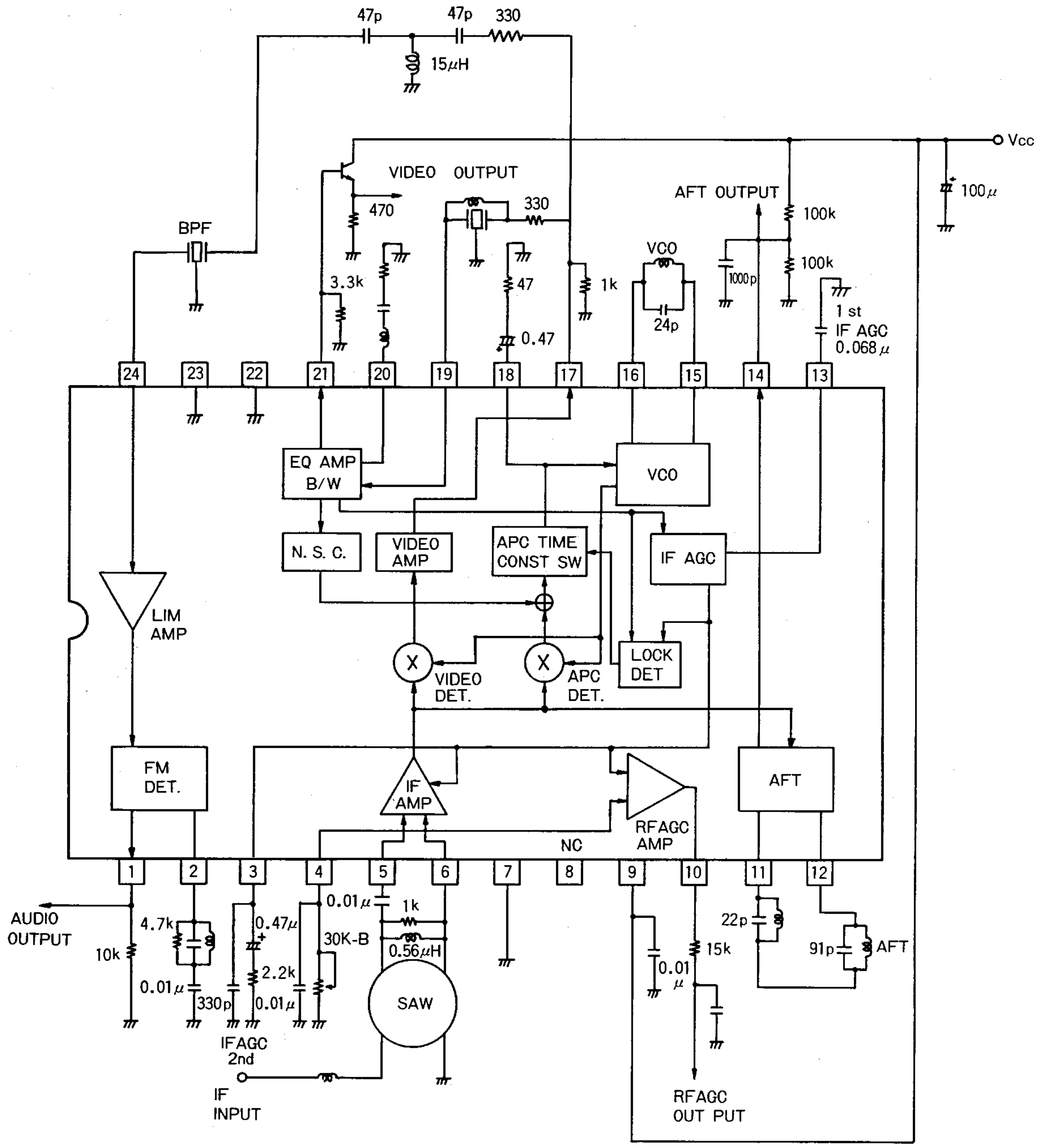
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Parameter	Symbol	Conditions	min	typ	max	Unit
AFT detection sensitivity	Sf		50	70	100	mV/kHz
VIF input resistance	Ri (VIF)	f = 58.75 MHz	0.8	1.3	1.75	kΩ
VIF input capacity	Ci (VIF)	f = 58.75 MHz		3.0	6.0	pF
APC pull-in range (U)	f_{PU}-2	S1 = ON	0.6	1.6		MHz
APC pull-in range (L)	f_{PL}-2	S1 = ON		–1.6	–0.8	MHz
VCO maximum variable range	Δf_U	V_{18} = 3 V, S1 = ON	0.6	1.6		MHz
	Δf_L	V_{18} = 7 V, S1 = ON		–1.6	–0.8	MHz
VCO control sensitivity	β	V_{18} = 5 V to 4.6 V	1.5	3.1	6.2	kHz/mV
SIF output signal voltage	V_O (SIF)	P/S = 20 dB	120	170	240	mVrms
[SIF Block] : V13 = 5 V						
SIF limiting sensitivity	Vi (lim)			33	39	dB/µV
FM detection output voltage	V_O		400	600	790	mVrms
AMR	AMR		40	49		dB
Distortion	THD			0.5	1.0	%
SIF S/N	S/N (SIF)		60	78		dB
[Mute Defeat]						
AFT defeat start voltage	VD_{11}		0.5	2.3		V
AV mute	V_{4TH}		0.5	1.9		V
FM mute	V_{2TH}		0.5	2.0		V
AFT defeat voltage	VD_{14}		5.4	6	6.6	V

Operating Characteristics at Ta = 25 °C, V_{CC} = 9 V

Parameter	Symbol	Conditions	min	typ	max	Unit
[VIF Block]						
Circuit current	I_9	V_{13} = 5 V, S1 = ON	36	41	49	mA
No-signal video output voltage	V_{21}	V_{13} = 5 V, S1 = ON	5.0	5.4	5.8	V
Maxinum RF AGC voltage	V_{10H}	V_{13} = 7 V, S1 = OFF	7.6	8	8.4	V
Mininum RF AGC voltage	V_{10L}	V_{13} = 7 V, S1 = ON		0	0.5	V
No-signal AFT output voltage	V_{14}	V_{13} = 5 V, S1 = ON	2.6	4.5	6.0	V
Input sensitivity	Vi	S1 = OFF	37	43	49	dB/µV
Video output amplifude	V_O (video)	S1 = OFF	1.5	1.75	2.0	Vp-p
Sync signal tip voltage	V_{21} (tip)	Vi = 10 mV, S1 = ON	3.25	3.55	3.85	V
Maximum AFT voltage	V_{14H}		8	8.5	9.0	V
Minimum AFT voltage	V_{14L}			0.3	1.0	V
White noise threshold voltage	V_{WTH}		6.8	7.2	7.6	V
White noise clamp voltage	V_{WCL}		4.0	4.4	4.8	V
Black noise threshold voltage	V_{BTH}	S1 = ON	2.5	2.8	3.1	V
Black noise clamp voltage	V_{BCL}	S1 = ON	3.7	4.1	4.5	V
AFT detection sensitivity	Sf		30	43	60	mV/kHz
SIF output signal voltage	V_O (SIF)	P/S = 20 dB	90	130	180	mVrms
[SIF Block]						
FM detection output voltage	V_O	V_{13} = 5 V	400	600	790	mVrms
[Mute defeat voltage]						
AFT defeat start voltage	VD_{11}		0.5	1.6		V
AV mute	V_{4TH}		0.5	1.1		V
FM mute	V_{2TH}		0.5	1.9		V
AFT defeat voltage	VD_{14}		3.9	4.5	5.1	V

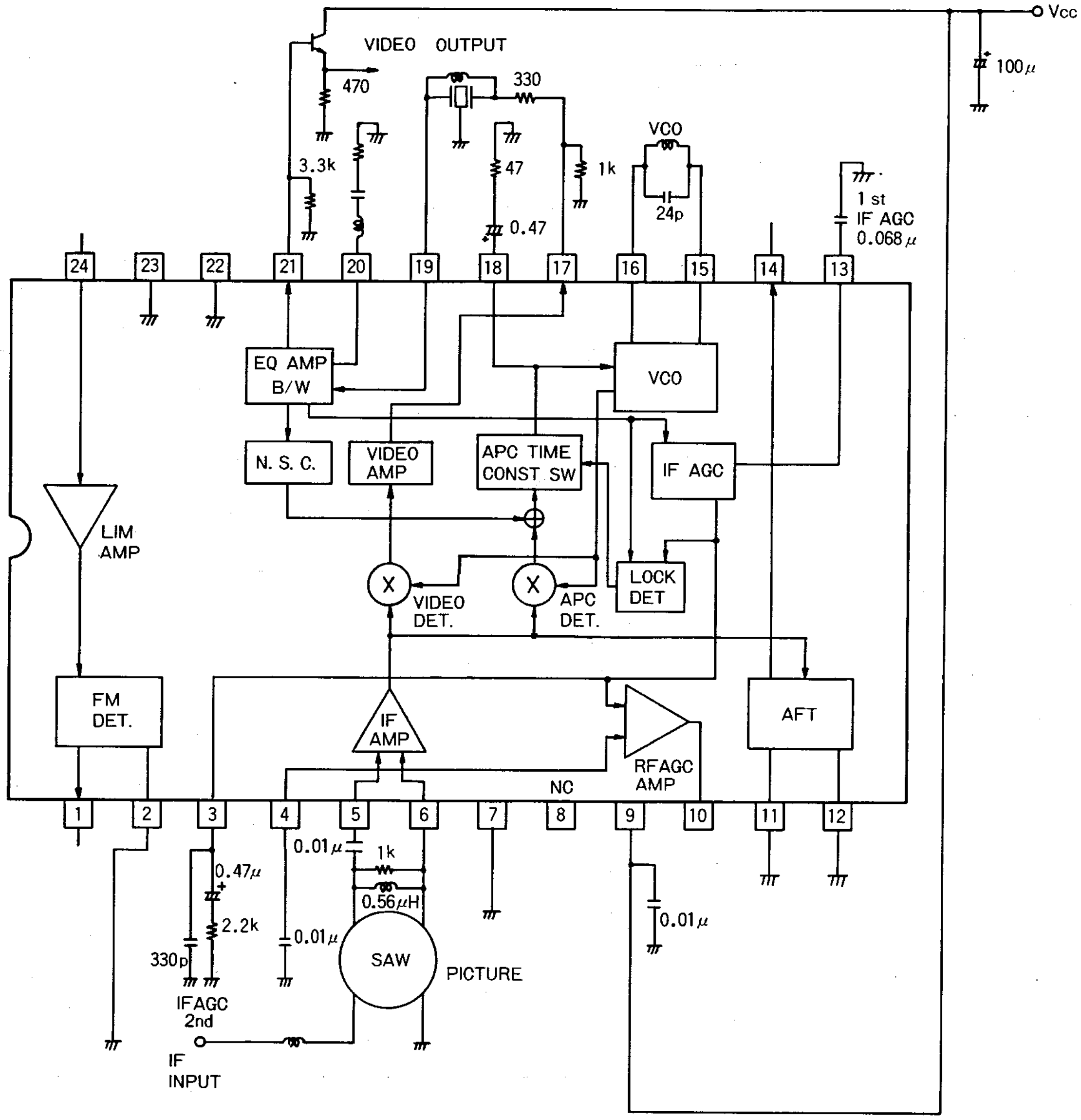
Sample Application Circuit (JAPAN)



Unit (resistance : Ω, capacitance: F)
Pins 22 and 23 are grounded inside the IC.

Sample Application Circuit (JAPAN)

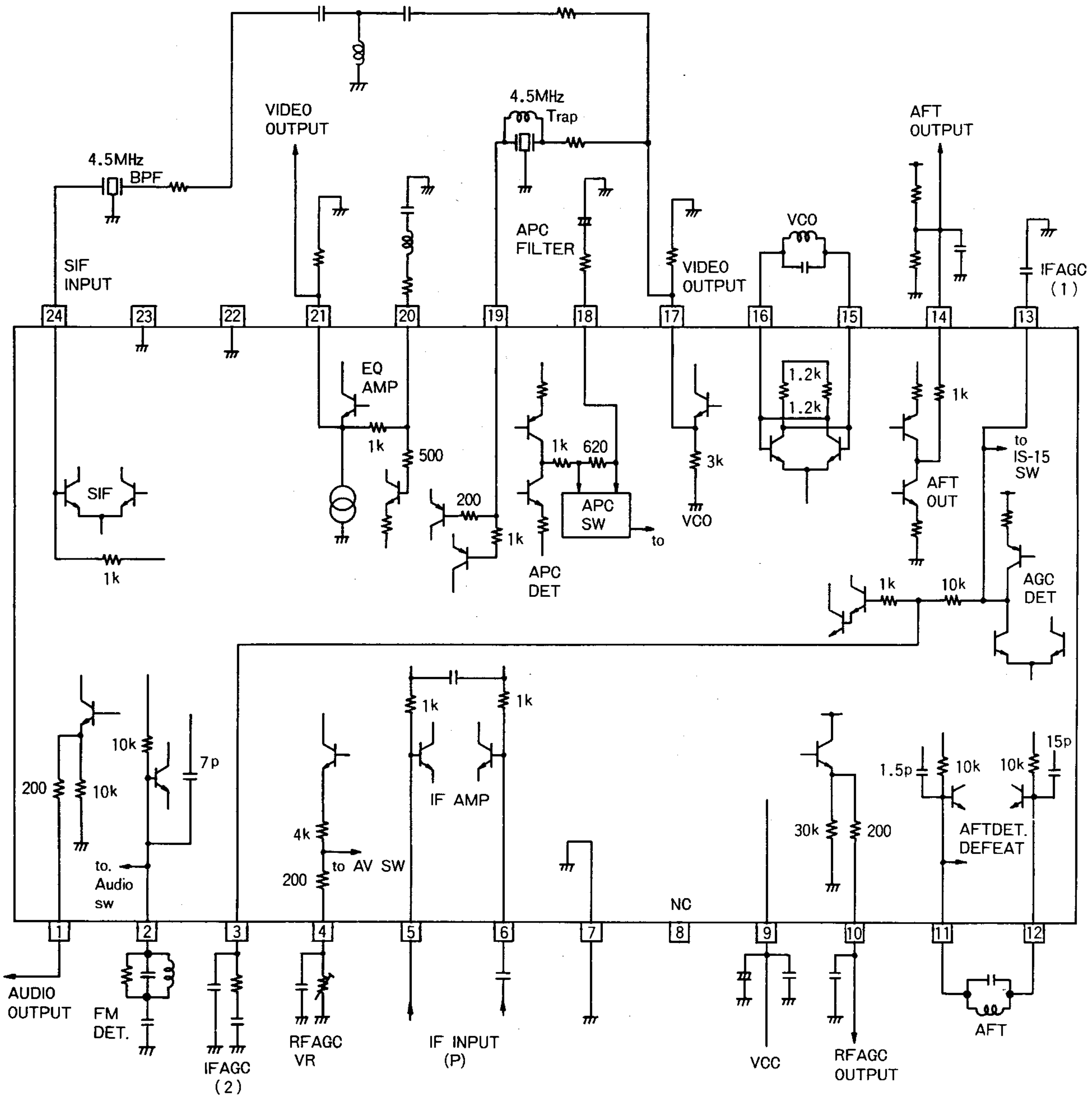
When using no SIF, 1stSIF, AFT, RFAGC.



Unit (resistance : Ω, capacitance : F)

1. When using no SIF circuit:
   - Pin1 = Open
   - Pin2 = GND
   - Pin24 = Open
2. When using no AFT circuit:
   - Pin11, 12 = GND
   - Pin14 = Open
3. When using no RFAGC circuit:
   - Connect a capacitor of 0.01 μF across Pin 4 and GND.
   - Pin10 = Open

LA7578N Interface Circuit



Unit (resistance : Ω, capacitance : F)

Buzz canceller

The LA7578N's PIF detector uses the PLL system. The PLL detection system has the following improved characteristics in comparison with the quasi-synchronous detection system.

(1) Better waveform response characteristics in comparison with the quasi-synchronous detection system.
(2) Harmonic components of the video signal are reduced.
(3) Improved 1/2 IF signal suppression ratio.
(4) Greatly reduced audio buzz.

In general, in the PLL detection system, if the VCO power supply is affected by noise such as flyback pulses (FBP), the VCO oscillating frequency can be disturbed by the noise component, with a worsening of the buzz characteristics as a result. Therefore, in order to protect against the effects of VCO power supply fluctuations due to this type of noise in the LA7578N, the VCO power supply has been regulated to be constant. The explanation below concerns the PLL detector. A typical PLL detection system consists of the blocks shown in Fig. 1.

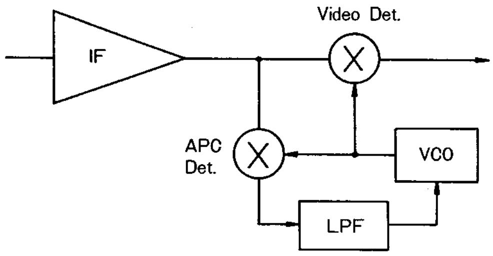


Fig. 1 PLL Detector

APC detection by the PLL detector shown in Fig. 1 is accomplished by multiplying the IF signal and the VCO signal by the phase difference π/2, generating the VCO control voltage. Multiplying by the phase difference π/2 makes it possible to suppress the AM component; in addition, because VCO is controlled through a low-pass filter (L.P.F), a carrier signal with a good C/N is obtained. As a result, by using the PLL detection system, the improved characteristics (1) through (4) listed above become possible.
However, because television broadcasts are transmitted using the vestigial sideband system, simply using the PLL detection system will create the following problems in regard to the audio characteristics. The RF signal that is input from the antenna is converted to an IF signal by the tuner, and a Nyquist strobe generated by a SAW filter is passed through the corresponding vestigial sideband . At this point, because the sideband in the region of the picture carrier is eliminated as shown in Fig. 2, the vector amounts of the upper sideband and the lower sideband differ, generating a phase distortion (θ) in the composite vector amount.

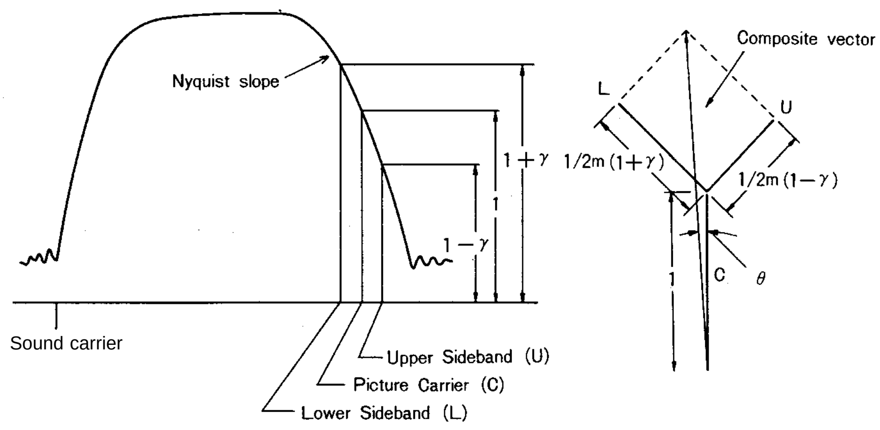


Fig. 2

If this phase distortion (θ) appears, the PLL VCO will be modulated in synchronization with the error voltage, which causes the generation of a buzz. At Sanyo, this buzz generated by the phase distortion (θ) is called ‘‘Nyquist buzz.’’ The LA7578N includes a new Nyquist buzz canceller circuit that suppresses this Nyquist buzz generated by the phase distortion (θ) in an effort to greatly improve the buzz characteristics. Fig. 3 shows the PLL detection system in the LA7578N, which uses this Nyquist buzz canceller circuit.

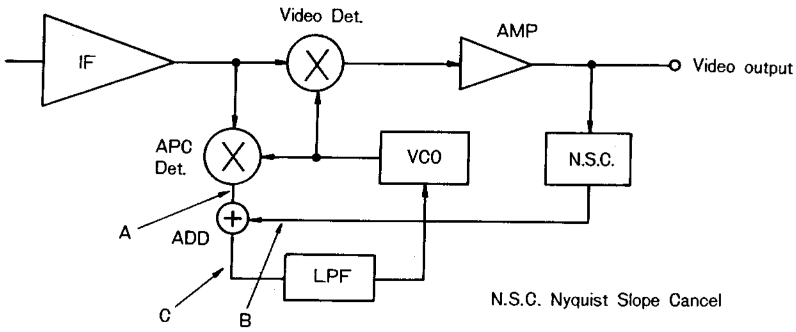


Fig. 3 PLL Detector with Nyquist Buzz Canceller

In the PLL detection system with the Nyquist buzz canceller, even if phase distortion such as that shown in A is generated, the phase distortion in the APC detection output can be eliminated by generating and adding in a quasi-reverse phase buzz signal.

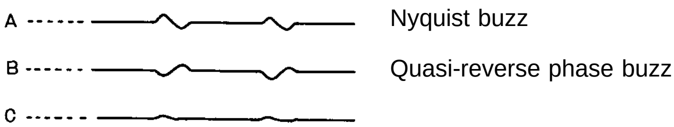


Fig. 4 Nyquist Buzz Canceller Waveforms

The effect of this Nyquist buzz canceller circuit is to broadly suppress the buzz (f_H harmonic) generated as a sideband of the SIF beat signal (4.5 MHz). As a result, great improvements can be made in regard to the buzz beat generated during demodulation of Japan audio multiplexing (L-R) and the buzz characteristics during demodulation of U.S. MTS (Multichannel TV Sound) (L-R). Furthermore, because this Nyquist buzz cancellation method has no effect on the time constant of the PLL loop, it is also possible to try to improve various characteristics, by making it possible to, for example, design an APC filter that is not readily affected by flyback pulses (F.B.P), etc.

Design Materials

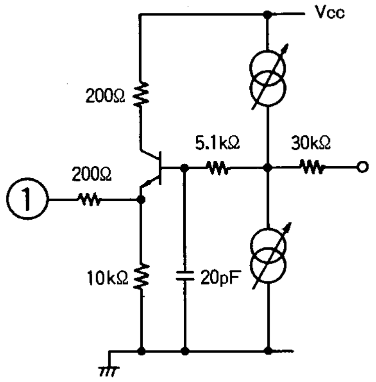


Fig. 5

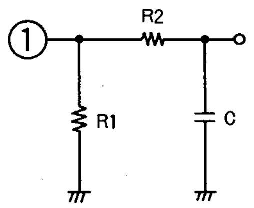


Fig. 6 De-emphasis

Pin 1 (FM detector output)

Pin 1 is the audio FM output pin. A 200Ω resistor is connected in series with the emitter follower.

(1) Audio multiplexing applications
Depending on the audio multiplexing decoder input application, the input impedance may be low, the L-R signals, etc., may be distorted, or the stereo characteristics may be degraded. In this type of situation, add a resistor between pin 1 and GND as shown in Fig. 6.
$R1 \geqq 5.1\ k\Omega$

(2) Monaural applications
Add a de-emphasis circuit with external CR.
$t = CR_2$

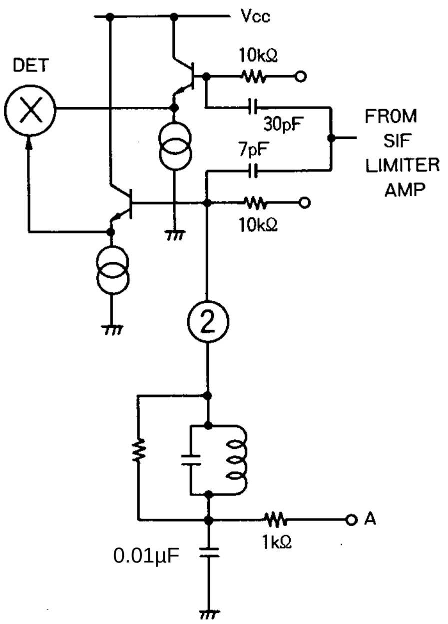


Fig. 7

Pin 2 (FM discriminator)

Pin 2 is the phase shifter pin for an FM quadrature detector. This pin generates the 90 deg phase shift signal needed for quadrature detection and adds it to the multiplier.

(1) The detector band characteristics are primarily determined by the coil Q and coil damping resistance. Determine the damping characteristics in accordance with the output level and band characteristics.

(2) When muting is applied, DC voltage (1 V or less) is applied to point A.

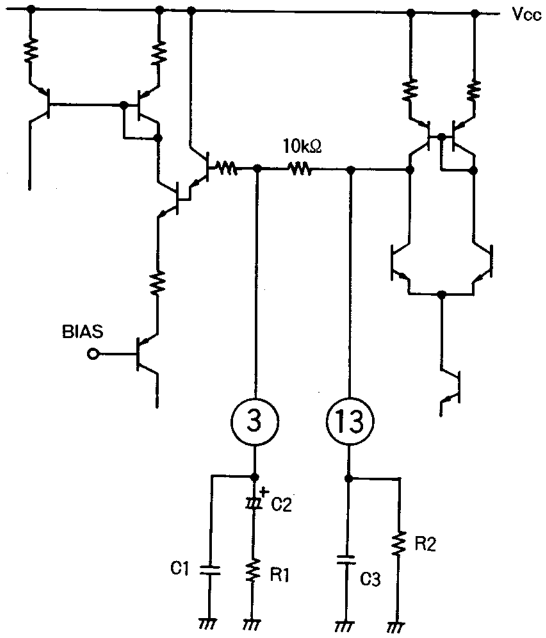


Fig. 8

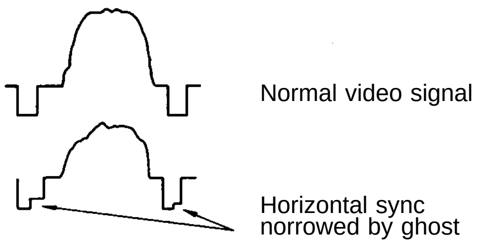


Fig. 9

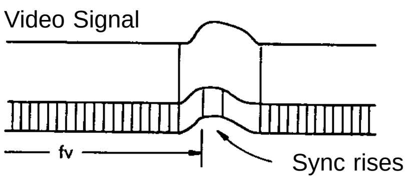


Fig. 10

Pins 3 and 13 (IF AGC pins)

Pins 3 and 13 are the IF AGC filter pins. The signal for which the peak was detected by the AGC detector is smoothed by pin 13 (1st AGC) and pin 3 (2nd AGC) to generate the AGC voltage. A signal which has passed through an audio trap is used for the video signal that is input to this IF AGC detector.

(1) These are typical AGC filter constants.

		Single time constant	Double time constant	Double time constant
Pin 3	C1	330 pF	330 pF	330 pF
	R1		2.2 kΩ	1.8 kΩ
	C2		0.47 µF	0.1 µF
Pin 13	C3	0.47 µF	0.068 µF	0.047 µF
	R2	820 kΩ	820 kΩ	820 kΩ

(2) Mute (IS-15 switch)
The black noise canceller can be cut by setting pin 13 to 1 V or less. When doing so, the AGC voltage must be applied to pin 3 from an external source to drive the AGC system. (IS-15 supported)

(3) Ghost problems
In a signal that produces ghosts, an interfering signal with a different phase overlaps with the desired signal, altering the video signal as shown in Fig. 9. The width of the sync signal narrows, making it impossible to maintain the IF AGC charge/discharge current ratio. If the phase change of the ghost interference wave increases, the symptom that appears is that the vertical sync portion rises as shown in Fig. 10. The countermeasure for alleviating this symptom is to insert a resistor (820 kΩ to 1 MΩ) between pin 13 and GND.

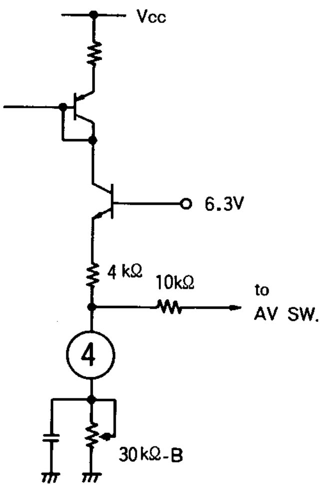


Fig. 11

Pin 4 (RF AGC VR)

Pin 4 is the RF AGC adjusting pin.
This pin sets the RF AGC operation point for the tuner.

(1) Mute
By setting this pin to 0.5 V or less, the FM output and the video output can be muted simultaneously.

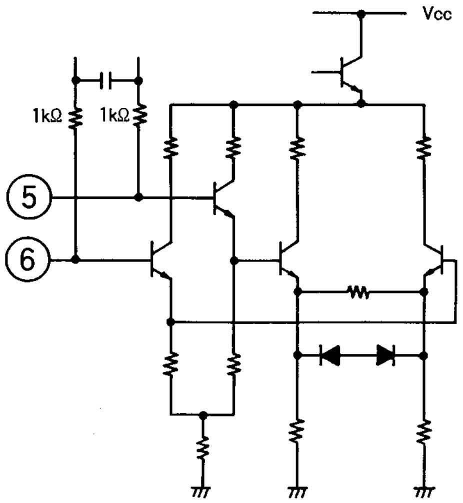


Fig. 12

Pins 5 and 6 (VIF input)

These are the VIF amplifier input pins. The inputs must always have their DC components eliminated with capacitors. The inputs are equilibrium inputs.
The input impedance is R ≒ 1.5 kΩ, C ≒ 3 pF.

Sanyo's SAW filter

There are two types of filters, depending on the piezoelectric substrate material.

(1) $LiTaO_3$ (lithium tantalate) SAW filters: TSF1xxx
TSF2xxx

While the $LiTaO_3$ SAW filters offer excellent stability with a low temperature coefficient of –18 ppm/ °C, the insertion loss is high. However, by using a coil, etc., for matching on the SAW filter output side (which does increase the number of external components), it is possible to suppress the insertion loss while at the same time making the level of the characteristics variable, which provides additional design freedom. (Refer to Fig. 13.)
In addition, because the SAW (surface wave) reflection is small, ripple within the band can be kept low.

(2) $LiNbO_3$ (lithium niobate) SAW filter: TSF5xxx

While the $LiNbO_3$ SAW filter has a high temperature coefficient of −72 ppm/ °C, it has a lower insertion loss by about 10 dB compared to the $LiTaO_3$ SAW filters. Therefore, matching on the output side of the SAW filter is not necessary. (Refer to Fig. 14.)
In addition, because the insertion loss is low (although the ripple within the band is somewhat higher than in the case of the $LiTaO_3$ SAW filter), the low impedance and small feedthrough diminish the effects of peripheral circuit components and the pattern layout, and make it possible to stabilize the trap characteristics outside of the band.

From the above, it is clear that the $LiTaO_3$ SAW filter is suitable for Japan and U.S. bands where the IF frequency is high, while the $LiNbO_3$ SAW filter is suitable for PAL and U.S. bands where the IF frequency is low.

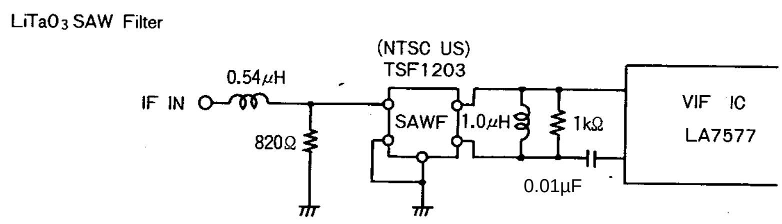


Fig. 13

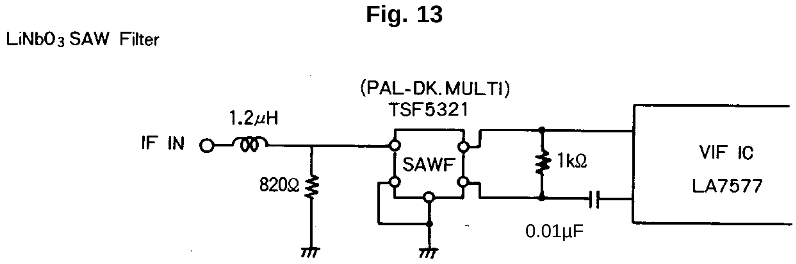


Fig. 14

Pin 8 (NC)

This is an NC pin.
When using the LA7577N, this pin becomes the 1st SIF input.

Pin 10 (RF AGC output)

Pin 10 is the RF AGC output pin.
This pin controls the tuner RF AGC. As shown in Fig. 17, a protective resistor of 200 Ω is connected in series with the emitter output. Determine the resistance bleeder value in accordance with the maximum gain of the tuner as shown in the diagram.

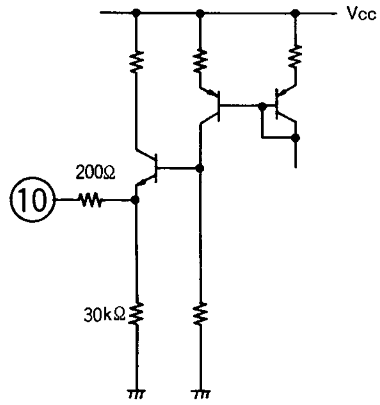


Fig. 15

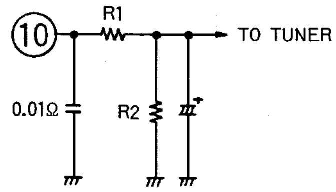


Fig. 16

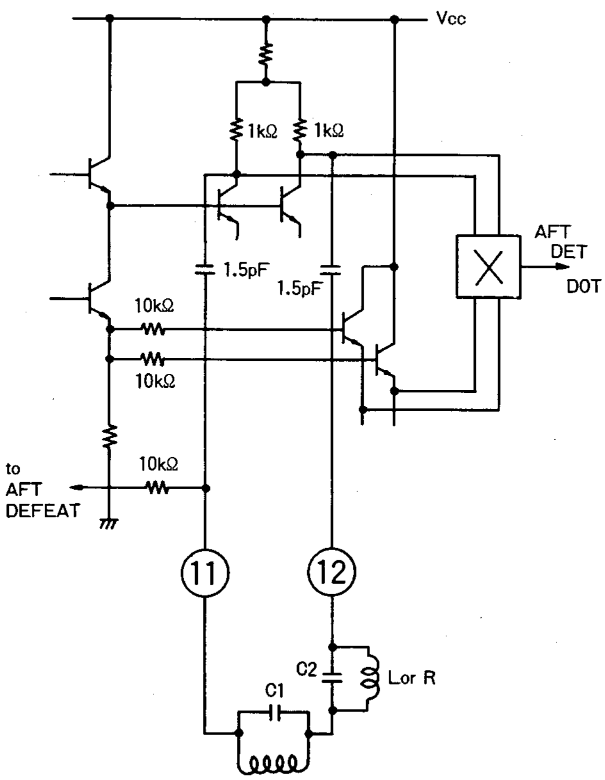


Fig. 17

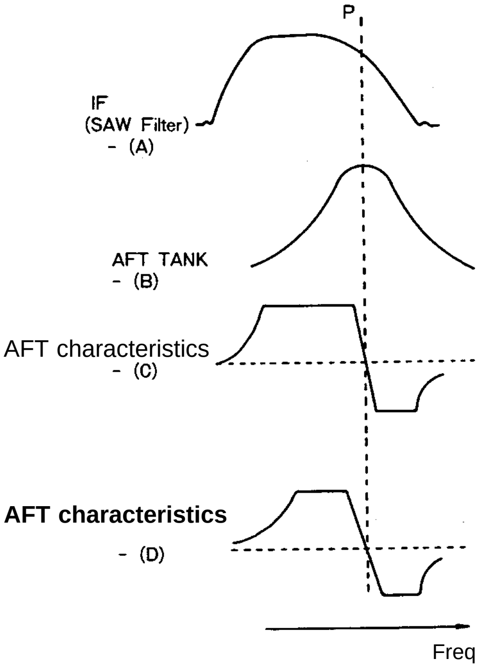


Fig. 19

Pins 11 and 12 (AFT coil)

Pins 11 and 12 are the AFT pins.

In the quadrature detection system, a signal that has been phase-shifted 90 deg is generated by an external AFT tank, and phase detection is done by the multiplier. The IF signal has the band characteristics shown in Fig. (A) because of the SAW filter. Accordingly, even if the band characteristics of the AFT tank change, the AFT characteristics are extended in the low band as shown in Fig. C, which makes misoperation more likely. As a result, band restrictions are placed on the low band frequencies as shown in Fig. D by inserting C2 in series with the AFT tank. The ratio between C1 and C2 needed in order to suppress misoperation should be about 5:1 (C1:C2). In this case, insert either a resistor or an L in parallel with C2 so that the DC balance of the AFT circuit is not disrupted.

(1) AFT DEFEAT
To implement AFT defeat, connect these pins to GND through resistor R1. The resistance used in this case is 20 kΩ or less.

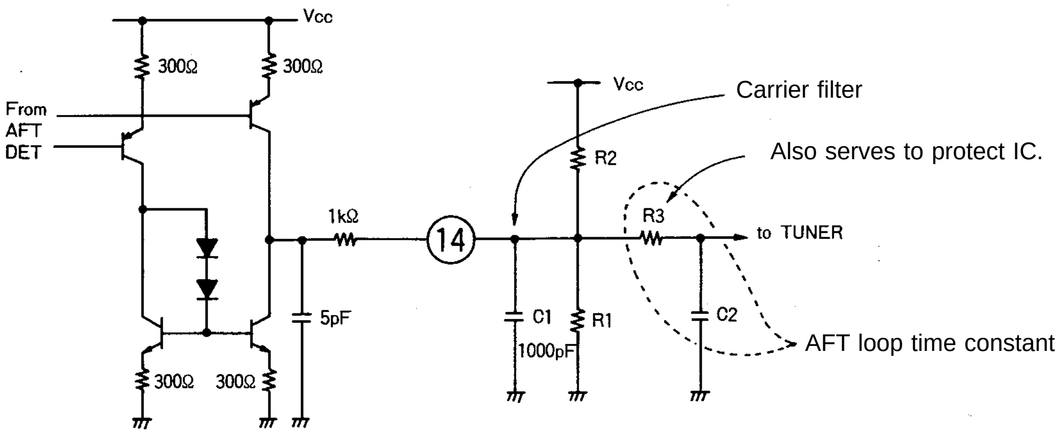


Fig. 18

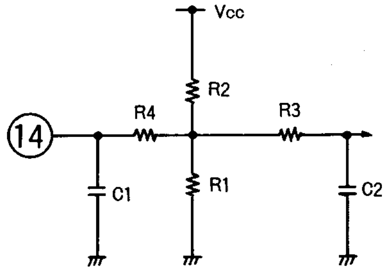


Fig. 20

Pin 14 (AFT output)

This is the AFT output pin.

This pin controls AFT of the tuner. The AFT voltage is generated by an external bleeder resistor. The AFT loop time constant is determined by inserting a resistor (R3) and a capacitor as shown in the diagram between this output pin and the AFT input pin of the tuner. This resistor also serves to protect the IC.

When the system of the selected station is the PLL system or the voltage synthesizer system, the variation of the no signal voltage of the AFT output becomes a problem. In this type of case, connecting a series resistor (R4) to the IC output as shown in Fig. 22 narrows the range over which AFT varies, making it possible to reduce the variation of the no signal voltage of the AFT output.

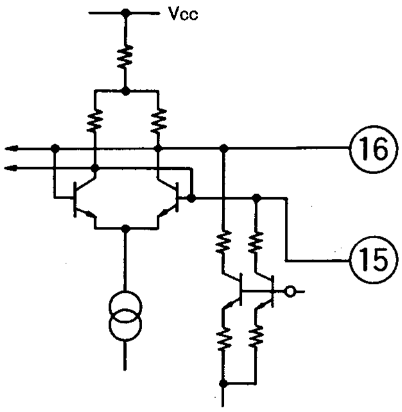


Fig. 21

Pins 15 and 16 (VCO tank)
These pins are for the VCO tank circuit.
The tank circuit capacitor is designed to be 20 to 27 pF. 24 pF is recommended. The VCO tank capacitor can be either built into the coil or a component in chip form. This circuit protects VCO from external influences.

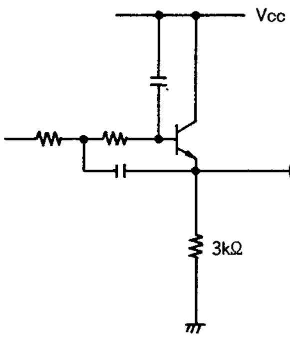


Fig. 22

Pin 17 (composite video output)
This is an output pin for the video signal including a 4.5 MHz component.
Although this is an emitter output, a resistor should be connected between pin 17 and GND in order to attain satisfactory drive capability.

V_{CC} = 12 V	R ≧ 1.2 kΩ
V_{CC} = 9 V	R ≧ 1 kΩ

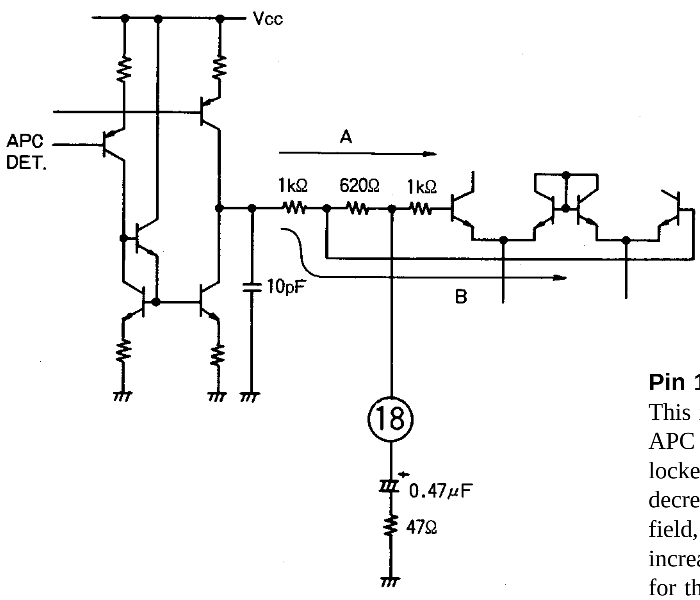


Fig. 23

Pin 18 (APC filter)
This is the APC filter pin.
APC time constant switching is performed within the IC. When locked, VCO is controlled by route A, and the APC loop gain decreases. When unlocked or when there is a weak electric field, VC is controlled by route B and the APC loop gain increases, broadening the pull-in range. The recommendations for this APC filter are: R = 47 to 150 Ω;
C = 0.47 μF.

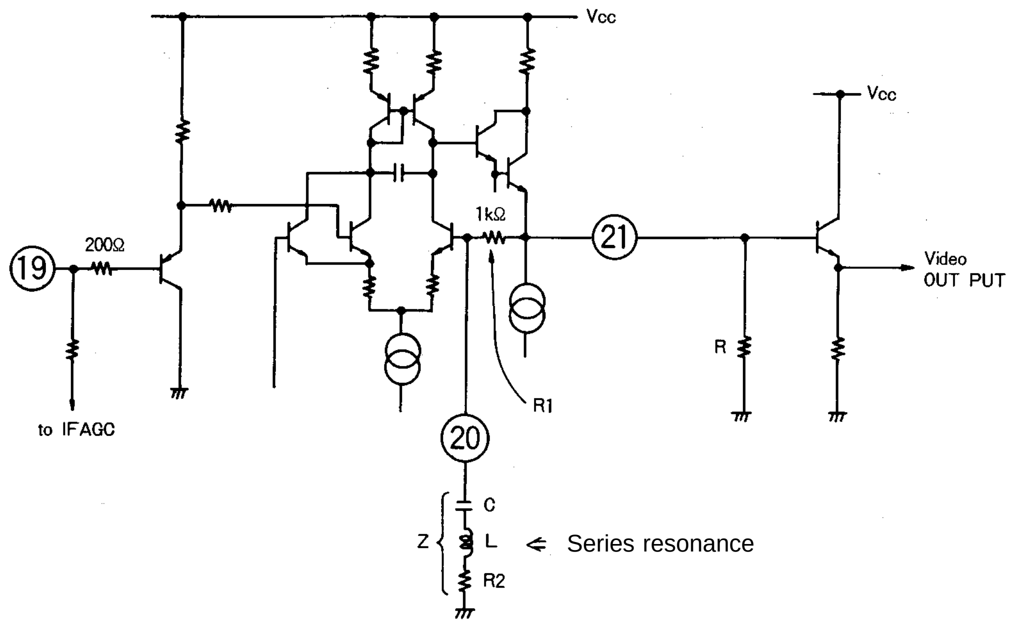


Fig. 24

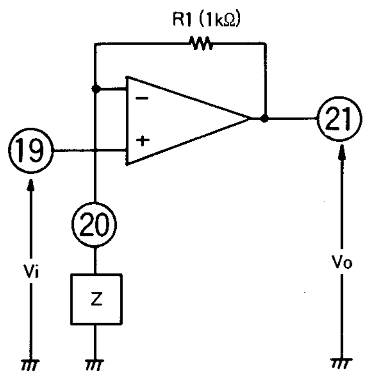


Fig. 25

Pins 19, 20, and 21 (EQ amplifier)

These pins are for the equalizer amplifier. A signal that has passed through a 4.5 MHz trap is input to pin 19 and is output from pin 21. Pin 21 is of emitter follower. A resistor must be connected between pin 21 and GND in order to attain satisfactory drive capability.

V_{CC} = 12 V	R ≧ 2.7 kΩ
V_{CC} = 9 V	R ≧ 2.2 kΩ

In addition, in order to draw the signal out externally, an external buffer transistor is required.

(1) Equalizer amplifier design

The equalizer amplifier consists of a voltage follower with a voltage gain of 0 dB. To compensate for the frequency characteristics, externally connect L, C, and R as shown in Fig. 26. Operation in this case is as follows:

Assigning the input to vi and the output to vo,

$(R1/Z + 1)(vi + vin) = vo$

Assuming imaginary short state,

if vin ≒ 0, then:

$Av = vo/vi = R1/Z + 1$

If the application of pin 20 is as shown in Fig. 27, it can be used as a voltage amplifier.

One point that requires caution, however, is the dynamic range of the equalizer amplifier. In short, the bleeder resistance ratio must be designed so that signals are not amplified excessively, and so that the leading edge voltage of the video signal sync signal is not too high or too low. In other words, the design must be such that the sync signal voltage does not change.

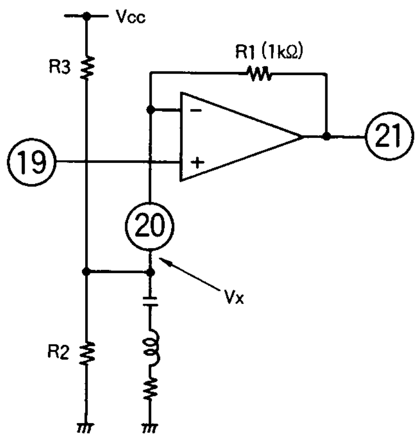


Fig. 26

Designing the external bleeder resistance ratio so that the output DC voltage (V21) does not change when the voltage is amplified by the equalizer amplifier

Assuming the desired gain is Av, then to make Vx ≒ V21 so that the sync signal voltage does not change:

$Vx = V_{CC} \times R2/(R2 + R3)$ .... : (1)
From the desired voltage gain:
$Av = 1 + 1\ k/Z1$ .... : (2)
$Z1 = R2 \times R3/(R2 + R3)$ .... : (3)
And then:
$R2 = 1\ k \times V_{CC}/[(V_{CC} - Vx) \times (Av-1)]$ ....: (4)
$R3 = 1\ k \times V_{CC}/[(Av - 1) \times Vx]$ ....: (5)
These simple calculations can be used to design the ratio.

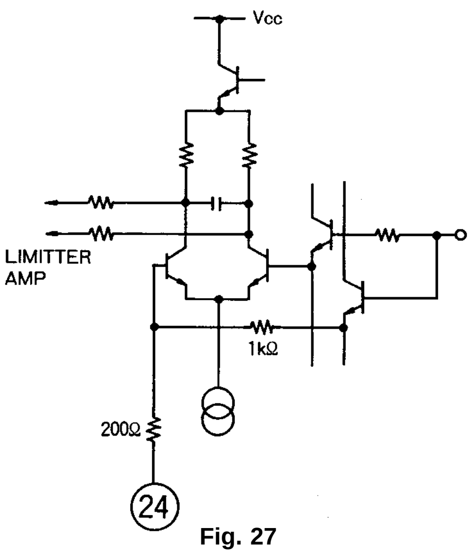


Fig. 27

Pin 22 (GND)
Connected to GND within the IC.

Pin 23 (GND)
Connected to GND within the IC.

Pin 24 (SIF input)
This is the SIF input pin.
The input impedance is approximately 1 kΩ. If an interfering wave (video signal, etc.) flows into this input, it will generate a buzz or buzz beat; therefore, caution must be exercised in regard to the pattern layout for the input circuit. Fig. (B) below shows a bad example.

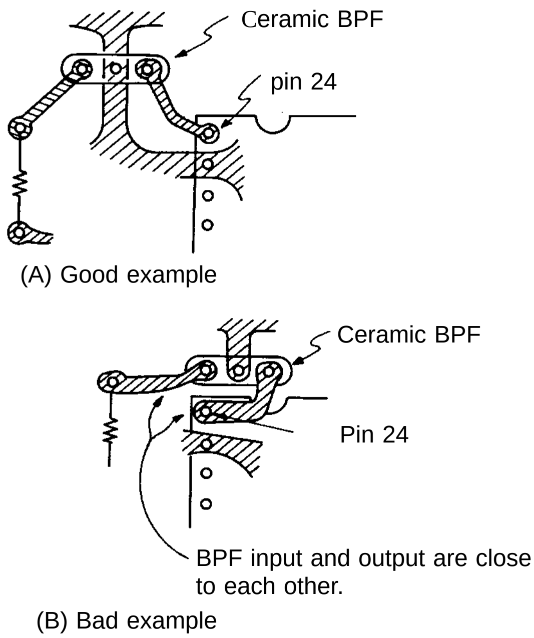
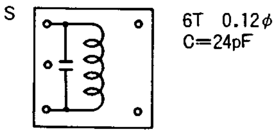
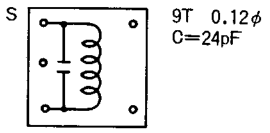
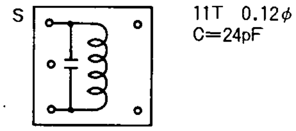
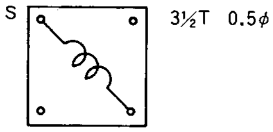
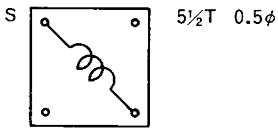
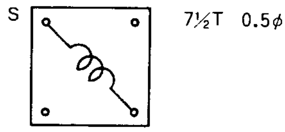
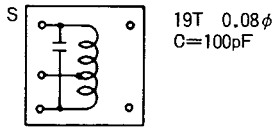
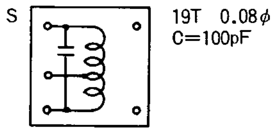
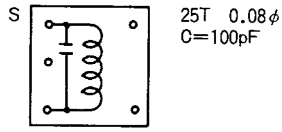


Fig. 28

Coil Specifications

	JAPAN f = 58.75 MHz	US f = 45.75 MHz	PAL f = 38.9 MHz
VCO coil T_1	 HW6226-4	 HW6227-4	 MA6389
AFT coil T_2	 MA8181	 MA6343	 MA7115
SIF coil T_4	 KS6102-1	 KS6102-1	 MA8182
SAW Filter (SANYO)	Picture TSF1110M M TYPE TSF1110P P TYPE TSF1141P P TYPE	Picture TSF1203M M TYPE TSF1239P P TYPE TSF1233P P TYPE	Picture (MULTI)TSF5321 K TYPE (BG) TSF5316U U TYPE (38M MULTI) TSF5341U U TYPE

(VCO tank circuit design considerations)

a. VCO tank circuit with an internal capacitor
When power is supplied to the IC, the heat from the IC is propagated to the PCB, and then to the VCO tank. In this instance, the legs of the tank coil substitute for a heat sink. Because the heat radiates from there, heat is not easily propagated to the VCO tank's internal capacitor, reducing the effect on VCO drift when the power is on.
Accordingly, it is desirable for the design to basically seek to cancel out the temperature characteristics through the L and C. Basically, it is best to use an L with a core material that has small temperature characteristics, and also to use a capacitor with small temperature characteristics.

b. VCO tank circuit with an external capacitor
In the case of an external chip capacitor, the heat from the IC is propagated to the PCB, and then to the external chip capacitor. As a result, the chip capacitor is affected by the heat, and its capacitance changes. In this case, because the VCO coil is relatively unaffected, the end result is that the alignment point of the VCO tank changes.
Accordingly, it is best to use an L with a core material that has small temperature characteristics, and also to use a capacitor with small temperature characteristics.